Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.623”**

****

**.492”**

**Top Material: Al**

**Backside Material: Pb/Sn/Ag**

**Bond Pad Size: G = .052” X .065” S = .060” X .060”**

**Backside Potential: DRAIN**

**Mask Ref: IX95**

**APPROVED BY: DK DIE SIZE .492” X .623” DATE: 10/19/16**

**MFG: IXYS THICKNESS .015” P/N: IXFD38N100Q2**

**DG 10.1.2**

#### Rev B, 7/1